

WHAT IS CLAIMED IS

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1. An apparatus, comprising:

a plurality of received-signal registers
which receive and store therein a plurality of
respective received-signal sequences;

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a selector which selects one of the
received signal sequences stored in said received-
signal registers;

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at least one code register which stores
therein a de-spreading-code sequence;

a multiplication circuit which multiplies
the selected one of the received-signal sequences by
the de-spreading-code sequence; and

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a summation circuit which obtains a sum of
results of the multiplication to obtain a
correlation between the selected one of the
received-signal sequences and the de-spreading-code
sequence.

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2. The apparatus as claimed in claim 1,
wherein said at least one code register includes a
plurality of code registers which store therein a
plurality of respective de-spreading-code sequences,
and said apparatus further comprising a selector
which selects one of said plurality of code
registers to select and supply the de-spreading-code
sequence to the multiplication circuit.

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3. The apparatus as claimed in claim 1,
further comprising:

- a delay-profile-holding unit which
generates a delay profile based on correlations
5 obtained by the summation circuit; and
- a path-timing-detection circuit which
detect a path timing by detecting a peak of the
delay profile.

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4. The apparatus as claimed in claim 3,
further comprising:

- 15 a first sequence-order-control circuit
which converts a single received-signal sequence
arranged in a first order into k received-signal
sequences arranged in a second order where k is more
than one, the k received-signal sequences being
20 supplied to said plurality of received-signal
registers; and
- a second sequence-order-control circuit
which converts the delay profile from one
corresponding to the second order to one
25 corresponding to the first order.

- 30 5. The apparatus as claimed in claim 4,
wherein the single received-signal sequence has a
spreading factor m and an over-sample ratio that is
equal to k, and each of the k received-signal
sequences has m samples therein, and wherein each of
35 said plurality of received-signal registers has m
stages.

6. The apparatus as claimed in claim 1,
further comprising:

N received-signal-holding units which hold
therein N received-signal sequences;

5 a selector which successively selects one
of said N received-signal-holding units, and
supplies the successively selected one of the N
received-signal sequences to said plurality of
received-signal registers at a speed N times faster
10 than sampling speed of the N received-signal
sequences;

N delay-profile-holding units which
generate N delay profiles corresponding to the N
received-signal sequences based on correlations
15 obtained by the summation circuit;

 a selector which successively selects one
of said N delay-profile-holding units, and supplies
the successively selected one of the N delay
profiles; and

20 a path-timing-detection circuit which
detect a path timing by detecting a peak of the
successively selected one of the N delay profiles.

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